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(54) Processor for converting pixel number of video signal and display apparatus using the same

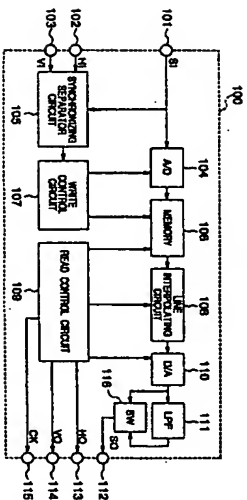
(57) A video signal processor which includes a circuit (109) for converting the number of lines in a digitized video signal, a circuit (109) for generating a display dot clock, a circuit (110) for outputting analog pixel data subjected to a line number conversion and having a frequency different from that of the display dot clock, and a circuit (111) for smoothing the analog pixel data; and in which a frequency of the display dot clock, an output frequency of the analog pixel data and a frequency

two of the horizontal synchronization signal satisfies an equation:

$$f_{dotN} = f_{dotM} \cdot \frac{M}{N}$$

where M and N are natural numbers satisfying $M \leq N$.

FIG. 1



Description

BACKGROUND OF THE INVENTION

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The present invention relates to a processor which receives a display video signal from a computer or the like and performs various sorts of processing operations over the signal according to specifications of a display device to display it on the display device.

A display video signal issued from an engineering workstation, a personal computer or a display terminal of a computer is output as a video signal of dots corresponding to picture elements or pixels on a display screen.

By converting the video signal into a digital signal and using a memory and an arithmetic operating circuit, the digital signal can be subjected to various processing operations including conversion of signal format of field frequency or aspect ratio and such image processing as enlargement/reduction (scaling), screen superposition or geometric transform. For example, when it is desired to form a 4-face multiscreen system in which 4 display devices are arranged adjacent to each other so that 2 of the 4 display devices are vertically in 2 stages and the remainder 2 are horizontally side by side and their 4 display screens are regarded as a single display screen, signals corresponding to 1/4 of an input video signal are subjected to a full-screen enlarging operation to display them at corresponding positions on the entire 4 screens. Thus, there can be arranged a display system which is large in scale and high in luminance and resolution. Output signals issued from these digital signal processing circuits are supposed to be displayed on a display device of a so-called multi-scanning cathode-ray tube (CRT) type, so that horizontal scanning frequency f_h , vertical scanning frequency f_v , display line number, etc. will vary depending on the format of the input signals and such signal processing contents as enlargement.

In these years, display devices of the conventional cathode-ray tube (CRT) type have been replaced by display devices of liquid crystal, plasma, LED, etc. These display devices have an advantage over the cathode-ray tube type display device that they can be made dimensionally small in depth and thickness with less occupation space and can have a large display screen. These display devices, however, have a problem that a coordinate system for representing respective pixels is fixed and thus cannot be changed. That is, in the display device of the fixed pixel number type, the numbers of horizontal and vertical display pixels (also sometimes referred to as pixel numbers, hereinafter) are fixed so that it is difficult to directly display a signal not conforming to the pixel numbers on the display device without subjecting to any operation. More in detail, it has been difficult to directly display a signal having 480 effective lines or a signal having 1024 horizontal effective pixels and 768 effective lines on a display device having 1280 horizontal pixels and 1024 vertical pixels.

For this reason, when it is desired to correctly display a signal having a pixel number different from that of a display device of the fixed pixel number type, a signal processing circuit for changing such a pixel number is heretofore required. For example, when it is desired to display a signal having 640 horizontal effective pixels on a display device of 1024 pixels, it is necessary to display 8 pixels with use of the 5 pixels of an input signal (640/1024=5/8) and thus to generate display pixels through interpolating operation of the input pixels. As methods for interpolating the pixels of a one-dimensional signal, there are known such algorithms as previous-value hold interpolation based on one nearest point, linear interpolation based on near 2 points, and convolution interpolation based on near 4 points. When these algorithms are applied to horizontal and vertical respectively, it is possible to convert the pixel numbers of a two-dimensional image.

Examples of the signal processing circuit for performing such pixel interpolating operation are disclosed in JP-A-5-294334 and JP-A-5-328194.

When these signal processing operations are carried out together with the conversion of signal format of field frequency and aspect ratio and with image processing operations including enlargement/reduction (scaling), screen superposition, and geometric transform, the numbers of horizontal and vertical pixels can be converted according to the display device for display therein.

However, these pixel number converting operations are required to be carried out at a higher speed as the display device is increased in its resolution. For example, when it is desired to display 1280 horizontal effective pixels and 1024 effective lines with a frame frequency of 60Hz, the dot clock becomes 100MHz or more. For the purpose of realizing such a high speed signal processing operation that the dot clock exceeds 100MHz, parallel processing operation is employed. The parallel processing operation is such that input pixels are separated into odd-numbered and even-numbered pixels, subjected to a converting operation to provide a double occupation time, and then are subjected to the parallel processing operation by 2 systems of processing circuits. In such a parallel processing system, it is highly difficult to perform arithmetic operation between adjacent pixel data, since pixels are processed as divided into odd-numbered and even-numbered pixel series.

Further, setting of an enlarging (reducing) factor (or scaling factor) requires data to be intermittently read out from a memory, but the data reading unit from the memory is limited by the number of parallel processing series (2 pixel units for the odd-numbered and even-numbered pixel series), which involves such a problem that it is impossible to freely set the enlarging (reducing) factor, thus making it difficult to perform the parallel processing operation.

For this reason, it becomes necessary to perform it with use of such a high-speed device as emitter coupled logic

(ECL). However, this involves a problem that this increases power consumption and the heat generation caused by the increased power consumption makes it difficult to make the circuit small in size, with increased costs.

Further, when simplification of the interpolating algorithm and circuit leads to deterioration in the picture quality, it is difficult to provide a display device which can be made small in size with low costs and less power consumption to provide a high quality of picture.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a video signal processor which eliminates the need for provision of a high-speed signal processing circuit, produces an excellent quality of image, and has a pixel number converting function.

In accordance with the present invention, the above object is attained by performing arithmetic interpolating operation between vertical lines with use of digital signals and by performing interpolating operation between horizontal dots with use of analog signals based on a low pass filter.

Further, in order to realize the horizontal interpolating operation with use of analog signals, a relationship of equation (1) which follows should be satisfied among a conversion frequency f_{ck} of a digital/analog (D/A) converter circuit, a frequency f_{ck} of a clock CK to the display device, and a frequency f_{ho} of a horizontal synchronization signal HO to be issued to the display device.

$$f_{ck}/N = f_{ck}/M = f_{ho} \quad (1)$$

where, M and N are natural numbers.

Further, in order to fix characteristics of the above low pass filter, the dot clock to the display device is arranged to have a substantially constant frequency regardless of the format of the input video signal.

Furthermore, the above low pass filter are arranged to have such characteristics that a frequency band is limited to 1/2 or less of the frequency f_{ck} of the display dot clock CK.

When the number of horizontal effective pixels of the input video signal coincides with that of the display device, the above low pass filter is bypassed.

In the inline interpolating operation, a weight coefficient when 2 lines of data are to be added together as weighted is generated in accordance with a nonlinear function.

In accordance with the present invention, pixel number conversion can be realized without using a high-speed, large-power-consumption and digital signal interpolating circuit based on digital signals. Further, vertical pixel interpolation can be realized using digital signals without causing any deterioration of image quality.

In accordance with the signal processor of the present invention, signals having various resolutions can be displayed with less cost and power consumption on such a small-size display device of a fixed pixel number type as liquid crystal, plasma or LED.

When the signal processor of the present invention is employed, there can be provided a small-sized display device which produces a high quality of image with less power consumption and low costs.

BRIEF DESCRIPTION OF THE DRAWINGS

- Fig. 1 is a block diagram of a video signal processor in accordance with an embodiment of the present invention;
 Fig. 2 is a flowchart for explaining the effects of a low pass filter for horizontal pixel number conversion;
 Fig. 3 shows an embodiment of a clock generation circuit in a read control circuit;
 Fig. 4 shows another embodiment of the clock generation circuit in the read control circuit;
 Fig. 5 a further embodiment of the clock generation circuit in the read control circuit;
 Fig. 6 shows an embodiment of a line interpolation circuit in the present invention;
 Fig. 7 is an input/output characteristic diagram of a nonlinear function;
 Fig. 8 is a diagram showing conditions of a nonlinear function;
 Fig. 9 is an embodiment of an interpolation control circuit in Fig. 6;
 Figs. 10A and 10B are diagrams showing how lines are interpolated;
 Figs. 11A, 11B, 11C and 11D are graphs showing relationships between interpolation distance and weight coefficient;
 Fig. 12 is another embodiment of the interpolation control circuit in Fig. 6;
 Fig. 13 is an embodiment of a pixel interpolating circuit in the present invention;
 Fig. 14 is a block diagram of a video signal processor using the pixel interpolating circuit of Fig. 13;
 Fig. 15 is an example when the circuit of Fig. 1 is applied to a RGB signal processing circuit;
 Fig. 16 is a block diagram of another embodiment of the video signal processor of the present invention; and
 Fig. 17 shows an embodiment of a display device in which the video signal processor of the present invention is

provided.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be explained with reference to the accompanying drawings.

Fig. 1 is a block diagram of a video signal processor 100 in accordance with an embodiment of the present invention, which includes an input terminal 101 to which a video signal SI is applied from an engineering workstation, personal computer or the like, an input terminal 102 to which a composite synchronization signal HI containing a horizontal synchronization signal of the composite synchronization signal HI or horizontal or vertical synchronization information is applied, an input terminal 103 to which a vertical synchronization signal of the video signal SI is applied, an analog/digital (A/D) converter circuit 104 for converting the video signal SI to digital data, a memory 105 for writing therein the video signal converted to the digital data, a synchronizing separator circuit 105 for separating the synchronization signal contained in the input video signal SI or for waveform-shaping the synchronization signals received from the terminals 102 and 103, a write control circuit 107 for generating a write clock and a write control signal to be sent to the memory 106 on the basis of the synchronization information received from the synchronizing separator circuit 105, a line interpolating circuit 108 for converting the number of lines (also sometimes referred to as the number, hereinafter) to coincide with the number of lines of a display device, a digital/analog (D/A) converter circuit 110 for converting the video data read out from the memory 106 to an analog signal, a read control circuit 109 for generating a read control signal to be sent to the memory 106 and a read clock to be sent to the line interpolating circuit 108 and D/A converter circuit 110, a low pass filter (LPF) 111 for removing harmonics components from an output of the D/A converter circuit 110, an output terminal 112 for a video signal SO, an output terminal 113 for a horizontal synchronization signal HO of the output video signal SO, an output terminal 114 for a vertical synchronization signal VO of the output video signal SO, an output terminal 115 for the clock CK of the display device, and a change-over switch 116 for bypassing the LPF.

A video signal received at the terminal 101 is converted by the A/D converter circuit 104 to digital data and then written in the memory 106. At this time, a sampling clock for use in the A/D converter circuit 104 is generated by a phase-locked loop (PLL) part in the write control circuit 107 on the basis of the horizontal synchronization signal received from the synchronizing separator circuit 105.

Under control of the control signal received from the read control circuit 109, data in the memory 106 is read out to the line interpolating circuit 108 and then subjected to an interpolating operation of adjacent lines for the number conversion. The data subjected to the line number change is converted by the D/A converter circuit 110 to an analog signal, subjected by the low pass filter 111 to removal of unnecessary harmonics components, and then output from the terminal 112 as the output video signal SO.

The change-over switch 116 selectively switches between an output of the D/A converter circuit 110 and an output of the low pass filter 111 to output it from the terminal 112. When the number of horizontal effective pixels in the input video signal does not coincide with that of the display device, the change-over switch 116 selects the output signal of the low pass filter 111 to be output from the terminal 112 as the output signal SO. When the number of horizontal effective pixels in the input video signal coincides with that of the display device, on the other hand, the change-over switch 116 selects the output signal of the D/A converter circuit 110 to be output from the terminal 112 as the output signal SO. Thus, the video signal can be output from the output terminal SO to the display device without being subjected to the band restriction of the low pass filter 111. In this connection, the change-over control of the change-over switch 116 is carried out by a control circuit (not shown) externally provided, in substantially the same manner as the change-over of the pixel number of the input video signal.

The change-over switch 116 may be provided as necessary and thus in some cases, it can be omitted.

A dot clock signal necessary for the display device is output from the terminal 115.

These terminals 112, 113, 114 and 115 are connected directly to the display device or connected thereto through such an edit controller as a switcher to display the video signal processed by the signal processing circuit.

Explanation will next be made as to the specific operation, in the case where the signal processor of the present invention is connected to the display device which can display a signal of 1280 horizontal display pixel dots, 1664 total horizontal dots (including blanking dots), 1024 display effective lines, a total number 1078 of lines, a horizontal scanning frequency of 64.3KHz, a vertical scanning frequency of 60Hz and a dot clock frequency of 107MHz, so that a signal of 1024 horizontal effective pixels, 768 effective lines and a vertical scanning frequency of 70Hz is converted and displayed.

In this example, the effective line number can be increased to $4/3 (768/3 \times 4 = 1024)$ and the horizontal effective pixel number can be increased to $5/4 (1024/4 \times 5 = 1280)$, so that the input video signal can be fully displayed on the screen of the display device. The signal processor of the present invention performs converting operations by performing the line number conversion through digital processing operation of the line interpolating circuit 108 and by performing the horizontal pixel interpolation through change of the frequency of the read clock to thereby prolong or shorten a display occupation duration of one pixel.

The A/D converter circuit 104 performs its sampling operation based on the dot clock whose frequency coincides

with the effective pixel number of the input video signal, whereby data of 768 lines each having 1024 pixels is written in the memory 106. The image data read out from the memory 106 is sent to the line interpolating circuit 108 where the data is subjected to an interpolating operation to generate 4-line data from 3-line data, whereby the input signal of 768 lines is converted to a display signal of 1024 lines. The interpolating operation causes conversion of the input data to the output data of 1024 lines each having 1024 pixels. In this conjunction, the frequency fck of the read clock is set at 85.6MHz (= 107MHz/4/5). Blanking data of fields each having 54 lines with 309 pixels per line is attached to the data under control of the read control circuit 109, whereby the data is output to the display device as the video signal of a total of 332 of horizontal dots and a total of 1078 of lines. Through such processing operations, the output signal of the signal processor can have the horizontal scanning frequency fho of 64.3KHz (= 85.6MHz/2/332) and 1078 of lines, and thus it can be displayed in exactly the same manner as when a signal of originally 1280 x 1024 pixels is input directly to the display device. In this connection, the dot clock CK to the display device is generated from frequency-multiplying the horizontal synchronization signal HO to the display device by increasing 1664 times (that is, $64.3\text{KHz} \times 1664 = 107\text{MHz}$), and then supplied to the display device. When the clock CK is supplied to the display device, the device can repeat the video signal received from the signal processor as a signal having a total of 1664 of horizontal dots and 1280 of horizontal effective pixels and can display it thereon. At this time, when the video signal is previously subjected by the low pass filter 111 provided in an output stage to a band limitation to 1/2 or less (for example, 45MHz) of the sampling frequency of 107MHz, (which is equivalent to sampling with the clock CK received from the signal processor), the display device can prevent aliasing noise caused by harmonics components therein.

With such an arrangement, since such horizontal pixel interpolating operation as necessary in a high-speed signal processing on a dot clock basis, increase in power consumption and involved heat generation can be prevented, and the circuit can be economically made small in size. Further, the horizontal interpolating operation based on the analog filter as well as the vertical interpolating operation based on digital signals enable realization of a high quality of pixel number conversion.

At this time, memory read clock is required to be changed according to the format of the input signal and the pixel number of the display device, but in the present invention, the clock is generated by J/K (J and K being natural numbers) multiplying a stable-frequency signal of a crystal oscillator circuit provided within the read control circuit 109 through the phase-locked loop (PLL, J and K being able to be set by an externally-provided control circuit (not shown)). Alternatively, the clock CK to be sent to the display device may be generated by the crystal oscillator circuit or the PLL and the memory read clock may be generated by the PLL. In any case, any arrangement can be employed, so long as the equation (1) is satisfied among the frequency fck of the memory read clock ROCK, the frequency fho of the display dot clock CK to be sent to the display device, and the frequency fho of the horizontal synchronization signal HO to be sent to the display device.

When $f_{ck}=85.6\text{MHz}$, $N=332$, $f_{ho}=107\text{MHz}$, $M=1664$ and $f_{ho}=64.3\text{KHz}$ as in the embodiment of Fig. 1 are substituted into the equation (1), the above relationship is confirmed to be satisfied as expressed by an equation (2) which follows.

$$85.6\text{MHz}/1332 = 107\text{MHz}/1664 = 64.3\text{KHz} \quad (2)$$

In this case, the memory read clock frequency fck is the same as the conversion frequency of the D/A converter circuit 110.

Explanation will then be made as to the effect of the low pass filter 111 shown in Fig. 1 by referring to a waveform diagram of Fig. 2. In the drawing, (a) shows a memory read clock from the read control circuit 109, (b) shows a digital data input to the D/A converter circuit, (c) shows an output analog signal received from the D/A converter circuit 110, (d) shows a waveform of the output of the low pass filter 111, and (e) shows a display dot clock CK to be sent to the display device. The digital data (b) input to the D/A converter circuit 110 on a clock basis of the clock (a) is converted to an analog signal having an amplitude indicative of its data value. The waveform of the output of the D/A converter circuit has such consecutive rectangular pulses containing many sharp edges as shown by (c). When the output signal of the D/A converter circuit is applied to the low pass filter 111, the edge parts in the signal are smoothed through its band limitation, as shown by (d). As a result, even when sampling is carried out with the display dot clock CK (e) having a frequency different from that of the memory read clock in the interior of the display device, a good interpolated output can be obtained without sampling the unstable data of the edge parts.

When the horizontal effective pixel number of the input video signal is larger than that of the display device, the filter operates as an anti-aliasing filter.

The low pass filter may be made up of such passive elements as inductance, capacitance and resistor. Or, the filter may comprise an active filter using a high-speed operational amplifier. Alternatively, the filter may comprise an active filter whose cut-off frequency can be externally controlled and whose characteristics can vary with the memory read clock ROCK and the display dot clock CK.

The format of the input video signal is not restricted to the above one, but the pixel number, line number, etc., may be changed as necessary depending on the resistor setting by an external control circuit. In this case, the horizontal

and vertical interpolation and scaling factor are changed to convert the format to such a format as to allow the data to be always displayed on the display device.

For example, when it is desired to display an input signal of 640 x 400 pixels on a display device of 1280 horizontal display pixels or dots and 1024 display effective lines, the line number is changed to twice, 64 blanking lines are added, the memory read clock is set at 53.6MHz (= 107MHz/2), thereby provide a horizontally twice enlargement.

Although the output format of the video signal has been explained in connection with the 1280 x 1024 pixels, the present invention is not limited to the specific example. For example, in the case of a display device having another display pixel number, the format of the input video signal may be changed to a signal format suitable for the display device. In this case, the characteristic of the output stage low pass filter is changed according to the display dot clock CK. Alternatively, when the characteristic of the low pass filter is previously determined based on the possible highest display dot clock CK, so that when the display pixel number is small, the vertical frequency is increased to make the display dot clock CK equal to the highest display dot clock CK, which results in that the input signal having a plurality of resolutions can be connected to and displayed on the display device with use of a single system of low pass filter.

Explanation will next be made as to how to generate the clock of the read control circuit 109 in Fig. 1.

Shown in Fig. 3 is an arrangement of a clock generator provided in the read control circuit 109. The clock generator of Fig. 3 includes an oscillator circuit 13 such as a crystal oscillator for generating the memory read clock ROCK, a frequency divider circuit 14 for frequency-dividing the memory read clock ROCK by N to generate the horizontal synchronization signal HO, a phase comparison circuit 15 for comparing the phase of an output of a frequency divider circuit 16 with the phase of the horizontal synchronization signal HO, a voltage-controlled oscillator (VCO) 17 whose oscillation frequency is controlled by the phase comparison circuit 15, the frequency divider circuit 16 serving to frequency-divide the display dot clock CK received from the voltage-controlled oscillator (VCO) 17 by M and to input it to the phase comparison circuit 15.

The memory read clock ROCK generated by the oscillator circuit 13 is output to the memory 106, D/A converter circuit 110, etc., and is also output to the frequency divider circuit 14 to be frequency-divided thereby to generate the horizontal synchronization signal HO. The read control circuit reads data from the memory 106 on a line basis with respect to the horizontal synchronization signal HO as a reference. The phase comparison circuit 15, voltage-controlled oscillator (VCO) 17 and frequency divider circuit 16 form such a PLL that the output of the frequency divider circuit 16 applied to the phase comparison circuit 15 is equal to the horizontal synchronization signal HO with respect to the frequency, with the result that the PLL operates with the synchronized phase. Thus, the frequency fck of the dot clock CK corresponds to M times the frequency fho of the output horizontal synchronization signal HO, and the signal HO in turn corresponds to N division of the read frequency fck, whereby a clock satisfying the conditions of the equation (1) can be generated.

Although the read clock ROCK is generated by the frequency-fixed oscillator and the dot clock CK to be sent to the display device is generated by the PLL in the arrangement of Fig. 3, the dot clock CK to be sent to the display device may be generated by the frequency-fixed oscillator and the read clock ROCK may be generated by the PLL, an example of which is shown in Fig. 4.

Fig. 4 is arranged so that the oscillator circuit 13 generates the display dot clock CK and the frequency divider circuit 16 frequency-divides the dot clock CK by M to generate the horizontal synchronization signal HO. Through a PLL made up of the phase comparison circuit 15, voltage-controlled oscillator (VCO) 17 and frequency divider circuit 14, the frequency fck of the read clock ROCK is changed to a frequency corresponding to N times the frequency fho of the horizontal synchronization signal HO. As a result, similarly to Fig. 3, a clock satisfying the conditions of the equation (1) can be generated.

With such an arrangement as shown in Fig. 4, the display dot clock CK is set by an oscillator circuit such as a crystal oscillator to have always a constant frequency, so that, even when the format of the output video signal is changed, it is only required to change the vertical frequency and is unnecessary to change the characteristic of the low pass filter such as cut-off frequency in the foregoing arrangement example, whereby various formats of images can be displayed with use of a single system of filter. In this case, it is necessary to change the read clock ROCK according to the format of the output video signal, which can be realized by changing a frequency division ratio N of the frequency divider circuit 14 in Fig. 4, while the frequency of the read clock ROCK satisfies the conditions of the equation (1).

Next, another method for forming the clock generator in the read control circuit 109 will be explained by referring to Fig. 5.

The circuit of Fig. 5 includes a frequency divider circuit 18 for frequency-dividing a write clock WCK or another fixed clock signal to generate the horizontal synchronization signal HO, phase comparison circuits 15-1 and 15-2, voltage-controlled oscillator (VCOs) 17-1 and 17-2, and frequency divider circuits 14 and 16 having frequency division ratios of N and M, respectively. Through a PLL made up of the phase comparison circuit 15-1, voltage-controlled oscillator 17-1 and frequency divider circuit 16, the frequency fck of the display dot clock CK is changed to a frequency corresponding to M times the frequency fho of the horizontal synchronization output signal HO. Similarly, through a PLL made up of the phase comparison circuit 15-2, voltage-controlled oscillator 17-2 and frequency divider circuit 14, the frequency fck of the read clock ROCK is changed to a frequency corresponding to N times the frequency fho of the horizontal syn-

chronization output signal HO. As a result, as in Figs. 3 and 4, a clock satisfying the conditions of the equation (1) can be generated.

In any of the cases of Figs. 3, 4 and 5, the setting of the frequency division ratio of the frequency divider circuit, the oscillation frequency range of the voltage-controlled oscillator, etc. can be changed, that is, the setting change can be made by an externally-provided control circuit depending on the format of the input video signal or the contents of the signal processing.

Explanation will then be made as to the line interpolating circuit 108 in Fig. 1. The line interpolation circuit may comprise a conventional linear interpolation circuit but preferably comprise a line interpolation circuit using a nonlinear circuit to be explained below.

Referring to Fig. 6, there is shown a block diagram of an embodiment of a vertical line interpolation circuit in the present embodiment, which includes a buffer memory 1 for storing therein digitized input pixel data, a one-line delay circuit 2 for delaying a signal S1 read out from the buffer memory 1 and outputting it as a signal S0, an interpolation control circuit 3 for performing control over interpolation by setting an enlarging factor, a nonlinear circuit 4 for converting a weight coefficient received from the interpolation control circuit 3 to a nonlinear weight coefficient k according to a nonlinear function, a coefficient weighting circuit 5 for obtaining a weighted average of the signals S1 and S0 with the nonlinear weight coefficient k, a coefficient circuit 4' for outputting the nonlinear weight coefficient k, a coefficient circuit 501 for multiplying the input S1 by the nonlinear weight coefficient k received from the nonlinear circuit 4, a coefficient circuit 502 for multiplying the input S0 by the nonlinear weight coefficient 1-k, and an addition circuit 503 for adding together outputs of the coefficient circuits 501 and 502 and outputting the addition as an interpolated signal Ao.

An input video signal is stored in the buffer memory 1 as digital data. The buffer memory functions to accommodate a difference between data transmission rates caused by the pixel number conversion. The data S1 read out from the buffer memory is input to the one-line delay circuit 2 comprising a line memory or the like to allow simultaneous reference of the current target pixel data S0 and the pixel data S1 appearing one line later. The pixels of the data S0 and S1 are subjected by the coefficient weighting circuit 5 to the coefficient weighting operation with use of the nonlinear weight coefficient k received from the nonlinear circuit 4 to be output therefrom as the interpolated signal Ao which is expressed as follows.

$$Ao = S1 \cdot k + S0 \cdot (1-k) \quad (3)$$

where, $0 < k < 1$.

The weight coefficient α issued from the interpolation control circuit 3 is output as a value normalized so that a maximum distance between the line of the input signal S0 and a line to be interpolated (distance between the signals S0 and S1) is 1. For example, when it is desired to perform line interpolation at a position that a vertical distance ratio from the S0 is 3 and distance ratio from the S1 is 2, the interpolation control circuit 3 is arranged to output a weight coefficient α of 0.6 (= 3/(3+2)). Though the weight coefficient α is used as it is (without being subjected to the nonlinear conversion) as the weight of the weighted mean in the coefficient weighting circuit 5 in the conventional linear interpolation system, the nonlinear characteristic of the nonlinear circuit 4 causes conversion to the nonlinear weight coefficient k in the present invention, as follows.

For a constant A satisfying a relation of $0 < A < 0.5$,

if $\alpha < A$, then $k=0$

if $A \leq \alpha \leq 1-A$, then $k=(\alpha-A)/(1-2A)$

if $\alpha > 1-A$, then $k=1$

When $A=0.25$ as an example, the characteristic k is as follows.

IF $\alpha < 0.25$, then $k=0$

IF $0.25 \leq \alpha \leq 0.75$, then $k=2(\alpha - 0.25) \dots (4)$

IF $\alpha > 0.75$, then $k=1$

By applying such nonlinear transformation, if the position of the interpolation pixel is close to S0 ($\alpha < 0.25$), then $k=0$, and S0 is output as it is as the interpolated signal Ao. If the position of the interpolation line is close to S1 ($\alpha > 0.75$), then

$k=1$ and S1 is output as it is as the interpolated signal Ao. When it is desired to interpolate a line located nearly intermediate between S0 and S1 ($0.25 \leq \alpha \leq 0.75$), k increases from 0 to 1 as α is increased, S0 and S1 are subjected to the weighted average with use of this nonlinearly transformed weight coefficient and are output as the interpolated signal Ao.

In this way, by applying the nonlinear function to the weight coefficient of the coefficient weighting circuit 5, when the distance to the interpolation line is close, a movement of a center of balance of the pixel is allowed to prevent deterioration of the resolution of the edge parts; whereas, when the interpolation line is separated away from the input pixel line (in the vicinity of a middle point between the 2 lines), with the weighted averaging operation, smoothly interpolated outputs without any deflection of a center of balance of the pixel are obtained. As a result, there can be realized a line number converting function with less resolution deterioration and with less remained distortion in the graphics and character fonts.

Then explanation will be made as to the input/output characteristics of the nonlinear circuit 4 in Fig. 6, by referring to Fig. 7.

Fig. 7 is an input/output characteristic diagram showing a relationship of the value of an output k to an input α of the nonlinear circuit 4. The characteristic of the nonlinear circuit 4 is shown by a solid line in the drawing, whereas, a characteristic shown by a dotted line is a straight line for $k=\alpha$ and corresponds to a conventional characteristic based on the linear interpolation when the nonlinear circuit 4 is not used for comparison. As shown by the equation (4), the characteristic has 2 turn points at $\alpha=0.25$ and $\alpha=0.75$ and has a value k of 0 for $\alpha < 0.25$ and a value k of 1 for $\alpha > 0.75$ and linearly increases for $0.25 \leq \alpha \leq 0.75$.

The nonlinear circuit 4 can be easily implemented by preparing a look-up table with use of a read-only memory (ROM). That is, the input α is regarded as a ROM address and the value of the corresponding output k is previously written in the ROM as data.

Though two turn points are given for $\alpha=0.25$ and $\alpha=0.75$ in the equation (4) or in the characteristic of Fig. 7, the present invention is not limited to the specific example and the turn points may be given for $\alpha=0.3$ and $\alpha=0.7$. In this way, when the durations of the characteristic satisfying $k=0$ and $k=1$ are prolonged to steepen the slope of its central part of the characteristic curve, the characteristic of the interpolated output image becomes close to the characteristic of the nearest interpolation (previous value hold interpolation) to thereby suppress reduction in the resolution of the edge parts. Or when the turn points are given at $\alpha=0.2$ and $\alpha=0.8$, the ratio subjected to the interpolation of the central straight part becomes higher, whereby there can be obtained a smooth interpolated image close to the linear interpolation characteristic. The intended effects of the present invention can be obtained so long as a nonlinear function $k=f(\alpha)$ meets conditions which follow.

$$f(0) = 0 \quad (5)$$

$$f(1) = 1 \quad (6)$$

$$f(\alpha) = 1 - f(1-\alpha) \quad (7)$$

$$f(\alpha) \leq \alpha \text{ for } 0 < \alpha < 0.5 \quad (8)$$

$$f(\alpha) \geq \alpha \text{ for } 0.5 < \alpha < 1 \quad (9)$$

The equation (7) shows a condition required to maintain vertical (or horizontal) homogeneity of the interpolated characteristic and means a characteristic symmetric with respect to a center of coordinates (α, k)=(0.5, 0.5). The equation (8) shows a condition, when a distance to the interpolation pixel is small, required to make the weight coefficient smaller than that in the linear interpolation system to thereby suppress the resolution deterioration caused by the averaging operation.

The equation (9), which is also derived from the equations (8) and (7), shows a condition required to suppress the resolution deterioration. Another example of the nonlinear function satisfying the conditions of the equations (8), (9) and (7) is shown in Fig. 8. The characteristic curve is located within hatched zones in Fig. 8. When the characteristic curve is symmetric with respect to a point of coordinates (α, k)=(0.5, 0.5), the conditions of the equations (8), (9) and (7) can be satisfied. Any nonlinear function may be employed in the present invention, so long as it meets these conditions, which conforms to the subject matter of the present invention.

When the nonlinear function is applied to the weight coefficient in this way, there can be realized a pixel number converting function with less resolution deterioration and with less remarked distortion of graphics and character fonts. Explanation will next be made as to the arrangement of the interpolation control circuit 3 in Fig. 6, with reference to a block diagram of Fig. 9.

The circuit of Fig. 9 includes a register 301 for setting data for control of an enlarging factor, an addition circuit 302 for adding together a set value of the setting register 301 and an output of a D flip-flop array circuit 303 acting in latch

an output of the addition circuit 302 with the horizontal synchronization pulse signal HO, and a coefficient calculation circuit 304 for calculating the weight coefficient based on an interpolation distance D1S received from the D flip-flop array circuit 303. The setting register 301, addition circuit 302 and D flip-flop array circuit 303 are of an 8 bit type. Lower 8 bits of an addition output of the addition circuit 302 neglecting a carry signal are input to the D flip-flop array circuit 303, and the carry signal (9-th bit) is waveform-shaped and its output as the data read clock RCK from the buffer. The addition operation neglecting the carry means to perform addition with modulus 256 to show a residue obtained by dividing the arithmetic operation result by 256. The addition result as the output of the addition circuit 302 is delayed by the D flip-flop array circuit 303, and the output of the D flip-flop array circuit 303 is further added to the set value of the setting register 301, so that sequential cumulative addition is carried out by performing addition with modulus 256 over the register set value.

Explanation will next be made as to the operation of the interpolation control circuit 3 in Fig. 6, by referring to Figs. 10A and 10B. Numbers 1, 2, 3, ... in Fig. 10A represent input lines and a distance between the lines is 256. When it is desired to convert (increase) the number of input pixels to 483 times, interpolation lines are generated at intervals of 192 ($(256 \times 3/4)$) as shown by a, b, c, ... in Fig. 10B. In order to perform such control, the interpolation output interval 192 is set in the setting register 301 in Fig. 6 to perform sequential cumulative addition. The cumulative addition output D1S indicates a distance between the interpolation line S0 and interpolation line, e.g., 0, 192, 426, 64, ...; the coefficient calculation circuit 304 generates the weight coefficient on the basis of the received signal D1S. When the cumulative addition result exceeds 256 and carry takes place, a line update signal HINC generated from the carry signal causes data to be updated on a line basis from the buffer, thus updating the S0 and S1. The new S0 and S1 as well as lower 8 bits of the cumulative addition output can be used to generate an interpolation line.

Explanation will then be made as to the operation of the coefficient calculation circuit 304 in Fig. 6, with reference to Figs. 11A, 11B, 11C and 11D. Figs. 11A, 11B, 11C and 11D are examples of an input/output characteristic of the coefficient calculation circuit showing a relationship of the output interpolation coefficient to the input value D1S.

Fig. 11A shows the operation of the coefficient calculation circuit when arranged so that the coefficient linearly varies from 0 to 1.0 as the D1S is increased from 0 to 255.

Since the number of gray levels recognizable by human is generally about 100 to 200, a video signal I_n in many cases, represented by about 8 bits (R, G, B or Y, R-Y, B-Y respectively independently). For this reason, after subjected to an interpolating operation, the video signal is rounded eventually to about 8 bits, so that, even when interpolation coefficient is controlled in relatively rough steps, this has a less effect on image. Thus, the input/output characteristic of the coefficient calculation circuit 304 when the interpolation coefficient is controlled in 8 steps is shown in Fig. 11B. The interpolation coefficient α is controlled in 8 steps of 0, 1/8, 2/8 ($\alpha=1/4$), 3/8, 4/8 ($\alpha=1/2$), 5/8, 6/8 ($\alpha=3/4$), 7/8 and 8/8 (=1). Such an arrangement results in that the number of control bits of the coefficient circuit is reduced from 8 to 3 and the quality is reduced, there can be realized a processor which is made small in size, low in cost and high in image quality.

In this connection, the number of steps is not limited to the specific 8, but it may be arbitrarily set. When the step number is set at the power of 2, however, the structure of the coefficient circuit can be simplified with a combination of bit shift and adder.

In order to realize such a discrete output characteristic, it is merely required to set lower bits of the coefficient calculation circuit 304 at zero. More specifically, lower 5 of the 8 bits are all set at zero to be neglected and only the upper 3 bits are used to obtain 8-step discrete coefficients.

Fig. 11C shows an input/output characteristic in which $\alpha=0$ in a D1S range of 0 to 63, $\alpha=1$ in a D1S range of 192 to 255, and α varies linearly in a D1S range of 64 to 191.

In Fig. 11D, α steps linearly in a D1S range of 64 to 192 in Fig. 11C. That is, α is controlled in 8 steps of 0, 1/8, 2/8 ($\alpha=1/4$), 3/8, 4/8 ($\alpha=1/2$), 5/8, 6/8 ($\alpha=3/4$), 7/8 and 8/8 (=1).

Although $\alpha=0$ in the D1S range of 0 to 63, $\alpha=1$ in the D1S range of 192 to 255, and varies linearly in the D1S range of 64 to 191 in the operational characteristic of Fig. 11C, the present invention is not restricted to the specific example. For example, α may be 0 in the vicinity of the value of the D1S of 0, α may be 1 in the vicinity of the value of the D1S of 255, and may linearly vary in the vicinity of an intermediate value of the D1S.

As mentioned above, the enlarging operation of (256/N) times can be carried out based on the numeral value N set in the setting register 301. Though the setting register 301, addition circuit 302 and D flip-flop array circuit 303 have been of an 8 bit type in the arrangement of Fig. 6, the present invention is not limited to the specific example. For example, the arrangement of Fig. 6 may be of a 7 or 10 bit type. When the number of such bits is decreased, the circuit scale can be reduced. Further, an increase in the number of bits enables the enlarging factor to be set on a finer unit basis.

Shown in Fig. 12 is another embodiment of the interpolation control circuit 3 in Fig. 6, but which interior structure is modified. Other arrangement is substantially the same as that in Fig. 6. Explanation will be made as to the interior structure of the coefficient weighting circuit 5.

An arrangement of Fig. 12 corresponds to the coefficient weighting circuit 5 in Fig. 6, but which interior structure is modified. Other arrangement is substantially the same as that in Fig. 6. Explanation will be made as to the interior structure of the coefficient weighting circuit 5.

In the operation of the coefficient weighting circuit 5 arranged as shown in Fig. 6, the coefficient weighting circuit outputs the interpolated output line signal A0 in accordance with the equation (1) using the nonlinear weight coefficient

k converted by the nonlinear circuit. Reduction of the equation (1) to arrange it with respect to terms associated with the coefficient k results in an equation which follows.

$$A_0 = K \cdot (S1 - S0) + S0 \quad (10)$$

The arrangement of the coefficient weighting circuit 5 in Fig. 12 is based on the equation (10). In the arrangement, more in detail, a signal (S1-S0) is calculated by a subtraction circuit 504, multiplied by a coefficient circuit 501 by the coefficient k, and then added by an addition circuit 503 to the signal S0 to be thereby output as the interpolated output signal A0. That is, since the equation (1) is equivalent to the equation (10), even use of the coefficient weighting circuit 5 shown in Fig. 12 can produce effects similar to in the embodiment of Fig. 6.

When compared with the arrangement of Fig. 6, the addition/subtraction circuit is increased to 2 but the number of the control circuits is reduced to 1. A coefficient circuit for performing multiplying operation is, generally speaking, larger in scale than a subtraction circuit, so that, when the circuit is implemented with the arrangement of Fig. 12, the circuit scale can be made small in size.

Although the number of only vertical lines has been converted in both of the embodiments of Fig. 6 and 12, the present invention can be applied also to the conversion of the number of horizontal pixels. In the latter case, the one-line delay circuit 2 in Fig. 6 or 12 is replaced by a sample delay circuit to obtain an interpolated pixel output with use of data between adjacent pixels. Further, the interpolation control circuit 3 of Fig. 9 is arranged so that the horizontal synchronization pulses HO is replaced by the dot clock DCK and the line update signal HINC is replaced by the read clock RCK of the buffer memory 1.

When this is combined with the converting operation of the number of horizontal lines, there can be effected such two-dimensional processing as enlargement of the entire display screen or aspect ratio conversion. An embodiment in which the present invention is applied to the conversion of the numbers of horizontal and vertical pixels will next be explained by referring to Fig. 13.

In Fig. 13, reference numeral 12 denotes an example of circuit for performing the 2-dimensional pixel interpolating operation in accordance with the present invention. The circuit 12 includes a buffer memory 1 for storing therein digitized input pixel data, a line memory 6 for delaying a signal L1 read out from the buffer memory 1 by one line and outputting it, a vertical interpolation control circuit 3a for performing control based on setting of a vertical enlarging factor, a nonlinear circuit 4a for transforming a weight coefficient α received from the vertical interpolation control circuit 3a into a nonlinear weight coefficient k1 in accordance with a nonlinear function, a coefficient weighting circuit 5a for performing the weighted average of the signals L1 and L0 with use of the nonlinear weight coefficients k1 and (1-k1) received from the nonlinear circuit 4a, a one-sample delay circuit 2 for delaying by one sample the signal S1 received from the coefficient weighting circuit 4a, and outputting it as an output signal S0, a horizontal interpolation control circuit 3b for performing control operation based on setting of a horizontal enlarging factor, a nonlinear circuit 4b for transforming a weight coefficient α 2 received from the horizontal interpolation control circuit 3b into a nonlinear weight coefficient k2 in accordance with a nonlinear function, and a coefficient weighting circuit 5b for performing weighted average of the signals S1 and S0 with use of the nonlinear weight coefficients k2 and (1-k2) received from the nonlinear circuit 4b and outputting a weighted average result as an interpolated signal.

In the arrangement of Fig. 13, a vertical interpolating circuit made up of the line memory 6, coefficient weighting circuit 5a, nonlinear circuit 4a and vertical interpolation control circuit 3a is connected in cascade with a horizontal interpolating circuit made up of the one-sample delay circuit 2, coefficient weighting circuit 5b, nonlinear circuit 4b and horizontal interpolation control circuit 3b. The buffer memory 1 functions to accommodate a difference in data transmission rate caused by the conversion of the numbers of horizontal and vertical pixels and the conversion of the number of lines, and is commonly used as both vertical and horizontal interpolation buffers. The data L1 issued from the buffer memory 1 is one-line delayed by the line memory 6 and then output therefrom as the signal L0. As a result, the signals L0 and L1 become vertically adjacent pixels and, when the signals are subjected to the weighting averaging operation with use of the nonlinear weight coefficient k1 received from the nonlinear circuit 4a, vertically interpolated data corresponding to one line can be obtained. This is different from the horizontally interpolating operation used so far, that is, the weight coefficient α 1 and nonlinear weight coefficient k1 are held during one line and updated whenever the line is changed. A control signal RCK1 issued from the vertical interpolation control circuit 3a is for controlling the data update on a line basis. When this signal is not issued, the data of the identical line is repetitively output.

The data update of the buffer memory 1 and line memory 6 on a sample basis is controlled by a control signal RCK2 issued from the horizontal interpolation control circuit 3b.

The output signal S1 of the coefficient weighting circuit 5a after subjected to the vertical interpolating operation is one-sample delayed by the one-sample delay circuit 2 so that the pixels S0 and S1 horizontally adjacent on the display screen can be simultaneously referred to. As in the exemplary circuits of Figs. 6 and 12, the 2 adjacent pixels are subjected by the coefficient weighting circuit 5b to a horizontal interpolating operation with use of the nonlinear weight coefficient k2 received from the nonlinear circuit 4b and then output as an interpolated signal.

The characteristics of the nonlinear circuits 4a and 4b are set as shown in Fig. 7, as in the embodiments of Figs. 6

and 12.

With such an arrangement, the 2-dimensional operations including the enlargement of the entire display screen and the conversion of aspect ratio can be realized with less resolution deterioration and high image quality while suppressing distortion in graphics and character fonts. Further, the horizontal nonlinear characteristic may be different from the vertical one. For example, video signals of raster scans are made vertically discrete by scanning lines and tend to be susceptible to deterioration even when the vertical interpolation characteristic is close to the nearest (previous-value hold) interpolation characteristic. In the light of such characteristics, the vertical interpolation nonlinear characteristic is set to have turn points when $\alpha=0.3$ and $\alpha=0.7$, while the horizontal interpolation nonlinear characteristic is set to have turn points when $\alpha=0.25$ and $\alpha=0.75$. With such an arrangement, there can be realized a pixel number converting circuit which avoids deterioration of resolution caused by the vertical interpolation and produces a high quality of image. In this connection, the order of the horizontal and vertical interpolation circuits may be reversed as necessary.

Explanation will then be made as to an example of an arrangement of a signal processor which uses the pixel interpolating circuit 12 of Fig. 13 to convert signals of various image formats to signals conforming to such a display device of a fixed pixel number type as a liquid crystal display, by referring to a block diagram of Fig. 14.

In Fig. 14, the line interpolating circuit 108 in Fig. 1 has such an arrangement as shown in Fig. 13 and the low pass filter 111 and change-over switch 116 are not provided. Other constituent elements are the same as those in Fig. 1.

A video signal input from the terminal 101 is converted by the A/D converter circuit 104 to digital data and then written in the memory 106. At this time, a sampling clock used in the A/D converter circuit 104 is generated by a phase-locked loop (PLL) in the write control circuit 107 on the basis of a horizontal synchronization signal received from the synchronizing separator circuit 105, and the effective zone of the video signal is written in the memory 106.

The read control circuit 109, which incorporates an oscillator circuit such as a crystal oscillator for outputting a stable frequency, generates a horizontal synchronization signal HO, a vertical synchronization signal VO and a clock CK for display of the video signal on a display device of a fixed pixel number type. Under control of the control signals received from the read control circuit 109, the data within the memory 106 is converted by the pixel interpolating circuit 12 with respect to the numbers of lines and pixels, converted by the D/A converter circuit 110 to an analog signal, and then output from the terminal 112 as an output video signal SO. Further, the read control circuit 109 outputs, in addition to the horizontal synchronization signal HO and vertical synchronization signal VO, a clock CK for the display device requiring the dot clock, the clock CK being output from the terminal 115.

With such an arrangement, for example, a display signal of 1024 pixels x 768 lines can be displayed as enlarged display. Such processing is realized, for example, by the pixel interpolating circuit 12 which performs horizontal enlarging operation of 1.25 times ($1024 \times 1.25 = 1280$) and vertical enlarging operation of 1.333 times ($768 \times 1.333 = 1024$). Or this is realized, for the purpose of keeping a horizontal/vertical aspect ratio, by performing horizontal and vertical enlarging operations of both 1.25 times and by adding 64 blanking lines to vertical lines.

The memory 106 writes therein the effective zone of the input signal on a field basis and converts it with respect to field frequency. The memory 106 may be commonly used also as the buffer memory 1 in the pixel interpolating circuit 12 of Fig. 13. At this time, the reading operation from the memory 106 on a line basis is carried out according to the signal RCK1 received from the vertical interpolation control circuit 3a within the pixel interpolating circuit 12 of Fig. 13, while the reading operation on a dot basis is carried out according to the signal RCK2 received from the horizontal interpolation control circuit 3b. In this way, the common use of the memory enables reduction of the circuit scale.

With such an arrangement as mentioned above, even when the input signal does not coincide with the number of pixels required in a display device, the pixels can be number-converted and displayed without remarked deterioration of image quality. In this connection, the order of the memory 106 and the pixel interpolating circuit 12 in Fig. 14 may be reversed as necessary.

Although the conversion of the number of display pixels and the conversion of field frequency have been made in the explanation of the operation of Fig. 1, the respective control circuits may control their addresses to the memory or make the read clock frequency different from the write clock frequency in the course of writing and reading these data, thus realizing various image processings including scaling of image size.

In the embodiment of Fig. 1, a single system of video signal has been processed. Explanation will next be made as to an embodiment when 3 systems of color signals of red (R), green (G) and blue (B) are processed, by referring to a circuit arrangement of Fig. 15.

The circuit of Fig. 15 comprises 3 R, G and B systems each of which includes the video signal input terminal 101, A/D converter circuit 104, memory 106, line interpolating circuit 108, D/A converter circuit 110, low pass filter 111 and video signal output terminal 112 in Fig. 1. However, the change-over switch 116 is omitted herein.

The interior structures of the respective R, G and B systems are the same, and the constituent elements of the respective systems have the same reference numerals but added with R, G and B respectively. A/D converter circuits 104R, 104G, 104B, memories 106R, 106G, 106B, line interpolating circuits 108R, 108G, 108B, and D/A converter circuits 110R, 110G, 110B are controlled by the write control circuit 107 and read control circuit 109 common to the R, G and B systems. Applied to the synchronizing separator circuit 105 is, in addition to syn-

chronization input signals H1 and V1 independently of the video signal, a G input signal GI from a terminal 101G to cope with the synchronization signal multiplexed with a G signal. Other arrangement is substantially the same as that of Fig. 1. With such an arrangement as mentioned above, even color video signal including 3 signals of the R, G and B systems can be processed in substantially the same manner as in the foregoing embodiments.

When the numbers of horizontal and vertical effective pixels in the input video signal coincide with those of the display device, data sampled by the A/D converter circuit 104 is not subjected to any interpolating operation and output to the display device in a 1:1 relationship. In such a case, change-over switches 116R, 116G and 116B are provided for bypassing the low pass filters 111R, 111G and 111B.

Shown in Fig. 16 is another embodiment of the video signal processor 100.

The arrangement of Fig. 16 is different from that of Fig. 1 in that the order of the memory 106 and line interpolating circuit 108 is reversed.

That is, digital data issued from the A/D converter circuit 104 is subjected by the line interpolating circuit 108 to a line number conversion and then written in the memory 106. Since the line number conversion is carried out at the stage of writing it in the memory, the line interpolating circuit 108 is controlled by the write control circuit 107. Since the data written in the memory 106 is already subjected to the line number conversion, when it is desired to read the data from the memory 106, it is only required to convert the clock frequency to conform to the horizontal pixel number of a display device. With such an arrangement, when the number of effective lines of an input video signal is larger than that of the display device, the necessary capacity of the memory 106 can be made small. That is, at this time, the memory 106 performs vertical band limiting and line decimating operations.

In the foregoing embodiments, the signal processor of the present invention has been provided independently of the display device. Explanation will next be made as to an embodiment in which the signal processor of the present invention is built in a display device, with reference to Fig. 17.

In Fig. 17, reference numeral 100 denotes a signal processor of the present invention, numeral 10 denotes a display device, 9 denotes a display device of a fixed display pixel number type such as a liquid crystal display or a plasma display, 7 denotes a signal processing circuit for converting to signals necessary for the display apparatus 9, and 8 denotes a synchronization processing circuit for horizontal and vertical scan.

Video signals HO, BO and GO processed by the signal processor 100 of the present invention are subjected by the signal processing circuit 7 to conversion of voltages or currents necessary to operate the display device 9. A horizontal synchronization signal HQ, a vertical synchronization signal VO and dot clock CK issued from the signal processor 100 are applied to the synchronization processing circuit 8 to be processed to cause horizontal and vertical scan of the display device 9. More specifically, in the liquid crystal or plasma display device, driver operations are performed to determine X and Y coordinates.

With the aforementioned arrangement, incorporation of the signal processor within the display apparatus can advantageously economically eliminate the need for provision of an independent power supply and casing. In particular, the signal processor of the present invention performs its operation in a 1:1 relationship to the display apparatus, so that the incorporation of the signal processor in the display apparatus enables the suppression of increase in the number of wiring lines, thus realizing a display device having a high level of function.

It should be appreciated that the intention is not to limit the invention only to these embodiments shown but rather to include all alternations, modifications and equivalent arrangements possible within the scope of appended claims.

Claims

1. A video signal processor (100) comprising:

line number conversion means (108) for converting a number of lines in a digitized video signal; dot clock generation means (109) for generating a display dot clock having a predetermined frequency; analog data output means (110) for outputting analog pixel data subjected to a line number conversion and having a frequency different from that of said display dot clock; data smoothing means (111) for smoothing said analog pixel data; and synchronization signal generation means (109) for generating horizontal and vertical synchronization signals to be sent to a display device.

2. A video signal processor as set forth in claim 1, wherein said dot clock generation means, said analog data output means and said synchronization signal generation means issue output signals satisfying an equation;

$$f_{dotCK} = f_{dot} M = f_{ho}$$

where M and N are natural numbers satisfying $M \neq N$, f_{dot} denotes a frequency of said display dot clock, f_{ho} denotes an output frequency of said analog pixel data and f_{ho} denotes a frequency of said horizontal synchronization

tion signal.

3. A video signal processor as set forth in claim 1, wherein said data smoothing means includes means for limiting a band of the analog pixel data.
4. A video signal processor as set forth in claim 1, further comprising means (119) for switching to select analog pixel data smoothed or analog pixel data before smoothing and outputting a selected one.
5. A video signal processor as set forth in claim 1, wherein said line number conversion means includes means (1,2,501,502) for referring to signals of adjacent 2 lines and means (3,4,5) for generating interpolated signals from said 2 line signals.
6. A video signal processor as set forth in claim 5, wherein said interpolated-signal generation means (3,4,5) includes means (3) for calculating distances DIS between the 2 line signals and an interpolation line and means (4) for calculating an addition weight of the 2 line signals from said distances DIS on the basis of nonlinear conversion.
7. A video signal processor as set forth in claim 5, wherein said interpolated-signal generation means (3,4,5) includes conversion means based on a nonlinear function $f(x)$ satisfying relations:

$$f(x) = 0$$

$$f(x) = 1/(1-x)$$

$$f(x) \times x \times (0 < x < 0.5).$$
8. A video signal processor as set forth in claim 5, wherein said interpolated-signal generation means (3,4,5) includes conversion means based on a nonlinear function $f(x)$ satisfying relations:

$$\text{if } x < A, \text{ then } f(x) = 0$$

$$\text{if } A \leq x < 1-A, \text{ then } f(x) = (x-A)/(1-2A)$$

$$\text{if } x \geq 1-A, \text{ then } f(x) = 1.$$
9. A video signal processor as set forth in claim 8, wherein said constant A satisfies $0.2 \leq A \leq 0.3$.
10. A video signal processor comprising:
 - a line number conversion circuit (108) for converting a number of lines in a digitized video signal;
 - an analog data output circuit (110) for outputting analog pixel data based on digital video data subjected to a line number conversion;
 - a filter (111) for limiting a band of said analog pixel data; and
 - a clock generation circuit (109) for generating a horizontal synchronization signal, a vertical synchronization signal, and a display dot clock having a frequency different from an output frequency of said analog pixel data for display of an output signal of said filter.
11. A video signal processor as set forth in claim 10, wherein said dot clock generation means (109) issues output signals satisfying an equation:

$$f_{\text{dotCLK}} = f_{\text{CK}}/M = f_{\text{HO}}$$

where M and N are natural numbers satisfying $M \neq N$, f_{CK} denotes a frequency of said display dot clock, f_{HO} denotes an output frequency of said analog pixel data and f_{HO} denotes a frequency of said horizontal synchronization signal.
12. A video signal processor comprising:
 - a circuit (12) for converting at least one of the numbers of horizontal and vertical pixels in a digitized video sig-

nal in accordance with a nonlinear function;

- a circuit (110) for outputting analog pixel data based on digital video data subjected to said pixel number conversion; and
- a clock generation circuit (109) for generating a plurality of kinds of clock for display of said analog pixel data.
13. A display apparatus (Fig. 17) comprising:
 - line number conversion means (108) for converting a number of lines in a digitized video signal;
 - dot clock generation means (109) for generating a display dot clock having a predetermined frequency;
 - analog data output means (110) for outputting analog pixel data subjected to line number conversion and having a frequency different from that of said display dot clock;
 - data smoothing means (111) for smoothing said analog pixel data; and
 - means (7,8,9) for displaying said analog pixel data on the basis of said display dot clock.
14. A display apparatus as set forth in claim 13, wherein a frequency f_{CK} of said display dot clock, an output frequency f_{HO} of said analog pixel data and a frequency f_{HO} of a horizontal synchronization signal for display of said analog pixel data satisfy an equation:

$$f_{\text{dotCLK}} = f_{\text{CK}}/M = f_{\text{HO}}$$

where M and N are natural numbers satisfying $M \neq N$.
15. A display apparatus as set forth in claim 13, wherein said line number conversion means (108) includes means (1,2,501,502) for referring to signals of adjacent 2 lines and means (3,4,5) for generating interpolated signals from said 2 line signals.
16. A display apparatus (Fig. 17) comprising:
 - a line number conversion circuit (108) for converting a number of lines in a digitized video signal;
 - an analog data output circuit (110) for outputting analog pixel data based on digital video data subjected to line number conversion;
 - a filter (111) for limiting a band of said analog pixel data;
 - a clock generation circuit (109) for generating a horizontal synchronization signal, a vertical synchronization signal, and a display dot clock having a frequency different from an output frequency of said analog pixel data for display of an output signal of said filter; and
 - a display device (7,8,9) for displaying an output of said filter based on said display dot clock.
17. A display apparatus as set forth in claim 16, wherein a frequency f_{CK} of said display dot clock, an output frequency f_{HO} of said analog pixel data and a frequency f_{HO} of a horizontal synchronization signal satisfy an equation:

$$f_{\text{dotCLK}} = f_{\text{CK}}/M = f_{\text{HO}}$$

where M and N are natural numbers satisfying $M \neq N$.
18. A display apparatus (Fig. 17) comprising:
 - a circuit (12) for converting at least one of numbers of horizontal and vertical pixels in a digitized video signal in accordance with a nonlinear function;
 - a circuit (110) for outputting analog pixel data based on digital video data subjected to pixel number conversion; and
 - a device (7,8,9) for displaying said analog pixel data.
19. A video signal processor for interpolating a video signal discrete on a pixel basis and outputting interpolated signals as a one-dimensional video signal converted by horizontal/vertical scanning means, comprising:
 - hold means (1,2) for a plurality of pixels of an input original image in a buffer memory;
 - means (301-303) for finding interpolation distances between each pixel of the original image and output pixels to be interpolated;
 - control means (3) for controlling said hold means on the basis of said interpolation distances;

conversion means (4) for nonlinearly converting said interpolation distances; and generation means (5) for generating interpolated output pixels from adjacent pixels on the basis of nonlinearly-converted interpolation distances, wherein said interpolated output pixels are used as an output video signal discrete on the pixel basis.

20. A video signal processor as set forth in claim 19, wherein said conversion means includes means for performing its converting operation in accordance with a nonlinear function $f(x)$ satisfying conditions;

$$f(0) = 0$$

$$f(x) = 1 - f(1-x)$$

$$f(x) \leq x \quad (0 < x < 0.5).$$

21. A video signal processor as set forth in claim 19, wherein said conversion means includes means for performing its converting operation in accordance with a nonlinear function $f(x)$ satisfying conditions; for a constant A satisfying $0 < A < 0.5$,

$$\text{if } x < A, \text{ then } f(x) = 0$$

$$\text{if } A \leq x \leq 1-A, \text{ then } f(x) = (x-A)/(1-2A)$$

$$\text{if } x > 1-A, \text{ then } f(x) = 1.$$

22. A video signal processor as set forth in claim 21, wherein said constant A is equal to or higher than 0.2 and equal to or smaller than 0.3.

23. A video signal processor for 2-dimensionally interpolating a video signal discrete on a pixel basis and outputting interpolated signals as a one-dimensional video signal converted by horizontal/vertical scanning means, comprising:

hold means (1,2) for a plurality of pixels of an input original image in a buffer memory;

means (3a) for finding vertical interpolation distances between each pixel of the original image and output pixels to be vertically interpolated;

first control means (3a) for controlling the buffer memory of said hold means on a line basis on the basis of said vertical interpolation distances;

first conversion means (4a) for nonlinearly converting said vertical interpolation distances;

first generation means (6,5a) for generating vertically interpolated pixels from adjacent 2 line pixels on the basis of nonlinearly-converted vertical interpolation distances;

means (3b) for finding horizontal interpolation distances between said vertically-interpolated pixels and pixels to be horizontally interpolated;

second control means (3b) for controlling the buffer memory of said hold means on a pixel basis on the basis of said horizontal interpolation distances; and

second conversion means (4b) for nonlinearly converting said horizontal interpolation distances;

second generation means (2,5b) for generating horizontally interpolated output pixels from vertically-interpolated, adjacent 2 pixels on the basis of nonlinearly-converted horizontal interpolation distances,

wherein said horizontal interpolated output pixels are used as the output video signal discrete on the pixel basis.

24. A video signal processor as set forth in claim 23, wherein at least one of said first and second conversion means includes means for performing its converting operation in accordance with a nonlinear function $f(x)$ satisfying conditions;

$$f(0) = 0$$

$$f(x) = 1 - f(1-x)$$

$$f(x) \leq x \quad (0 < x < 0.5).$$

25. A video signal processor as set forth in claim 23, wherein at least one of said first and second conversion means includes means for performing its converting operation in accordance with a nonlinear function $f(x)$ satisfying conditions;

for a constant A satisfying $0 < A < 0.5$,

$$\text{if } x < A, \text{ then } f(x) = 0$$

$$\text{if } A \leq x \leq 1-A, \text{ then } f(x) = (x-A)/(1-2A)$$

$$\text{if } x > 1-A, \text{ then } f(x) = 1.$$

26. A video signal processor as set forth in claim 25, wherein said constant A is equal to or higher than 0.2 and equal to or smaller than 0.3.

27. A video signal processor as set forth in claim 19, wherein said generation means (5) includes means (501,502,503) for linearly adding horizontal or vertical pixel data at adjacent 2 points on the basis of nonlinearly-converted interpolation distances.

28. A video signal processor as set forth in claim 19, wherein said means for finding the interpolation distances between the pixel of said original image and the interpolation pixels includes means (301) for holding interpolation ratio data;

means (302,303) for performing cumulative addition of said interpolation ratio data with modulus N (N being an integer 2 or higher); and

means (303) for outputting the interpolation distances on the basis of said cumulative addition value.

29. A video signal processor as set forth in claim 23, wherein said first conversion means (6,5a) and said second conversion means (2,5b) have mutually different conversion characteristics.

30. A video signal processor as set forth in claim 23, wherein means (3a) for finding the interpolation distances in position between the pixels of said original image and the vertical pixels to be interpolated includes;

means (301) for holding vertical interpolation ratio data;

means (302,303) for performing cumulative addition of said vertical interpolation ratio data with modulus M (M being an integer of 2 or higher); and

means (303) for outputting vertical interpolation distances on the basis of cumulative addition values.

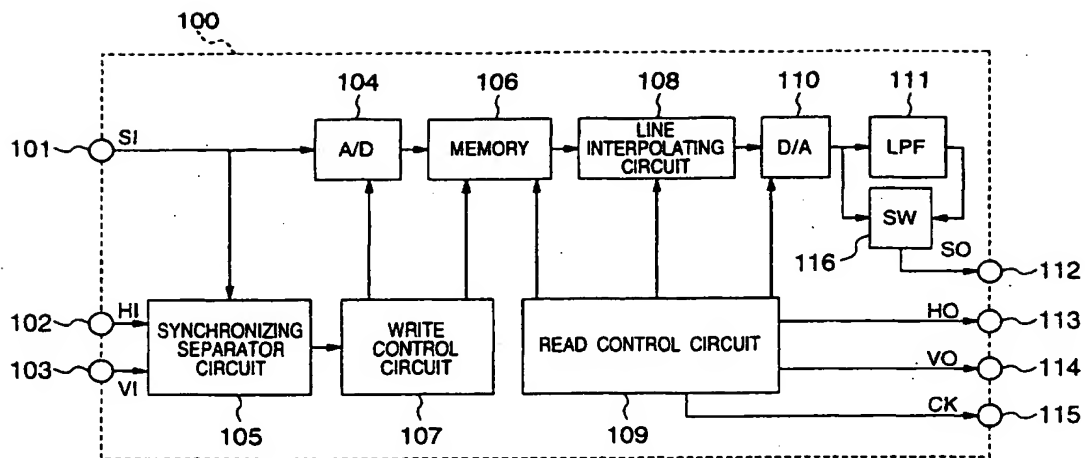
31. A video signal processor as set forth in claim 30, wherein said means (3b) for finding horizontal interpolation distances in position between said vertically-interpolated pixels and pixels to be horizontally interpolated includes;

means (301) for holding a horizontal interpolation ratio data;

means (302,303) for performing cumulative addition of said horizontal interpolation ratio data with modulus N (N being an integer of 2 or higher); and

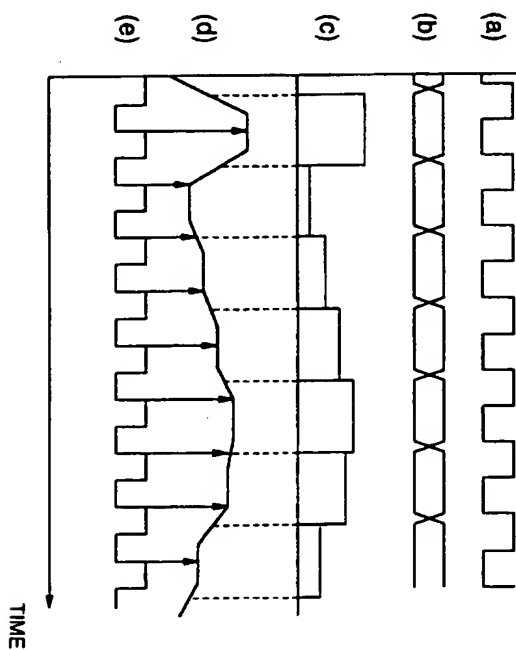
means (303) for outputting horizontal interpolation distances on the basis of cumulative addition values.

FIG.1



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FIG.2



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FIG.3

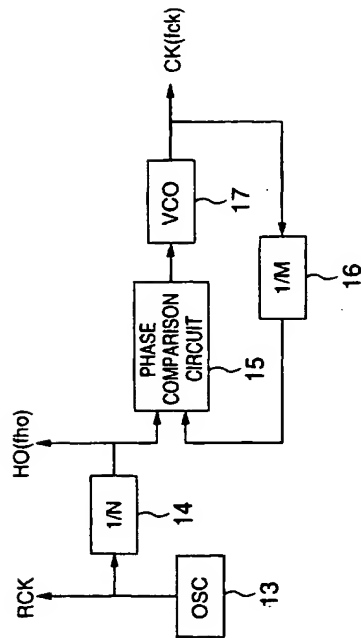


FIG.4

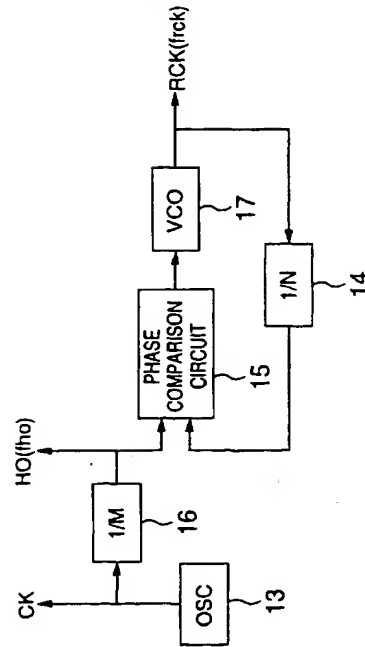


FIG.5

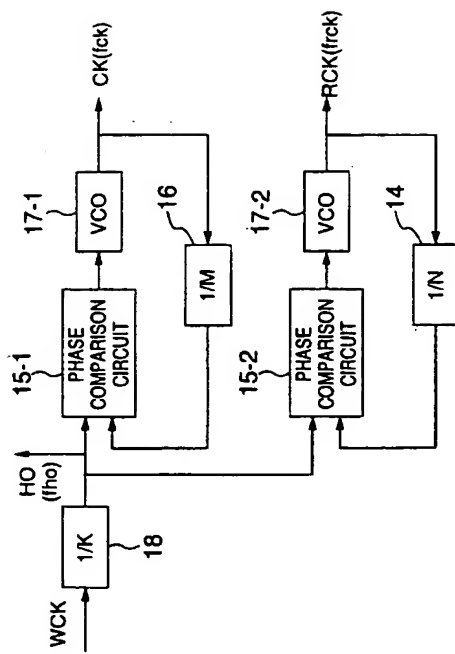
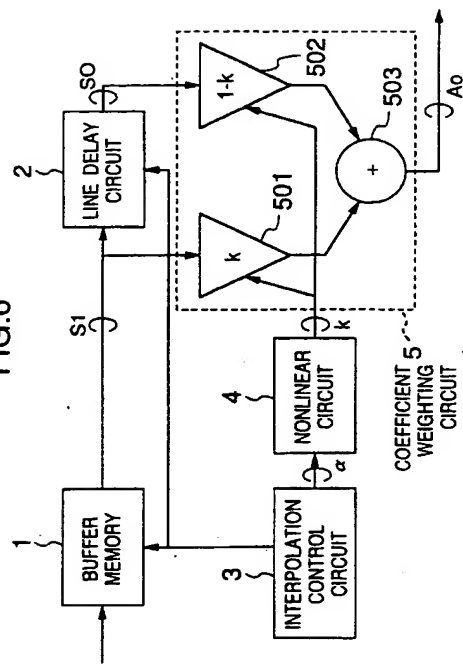


FIG.6



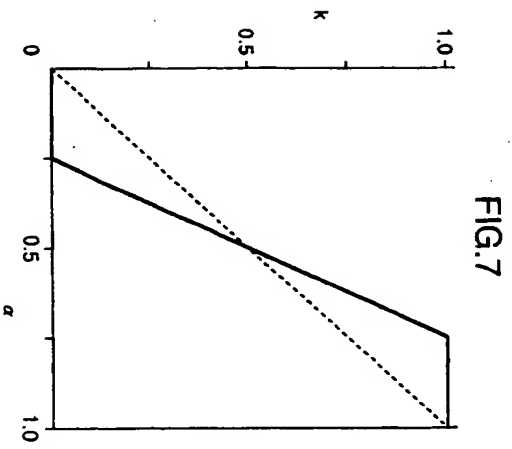


FIG. 7

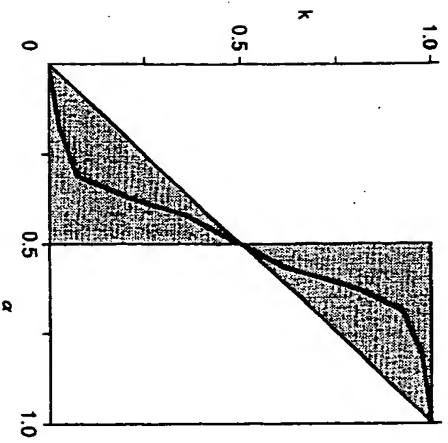


FIG. 8

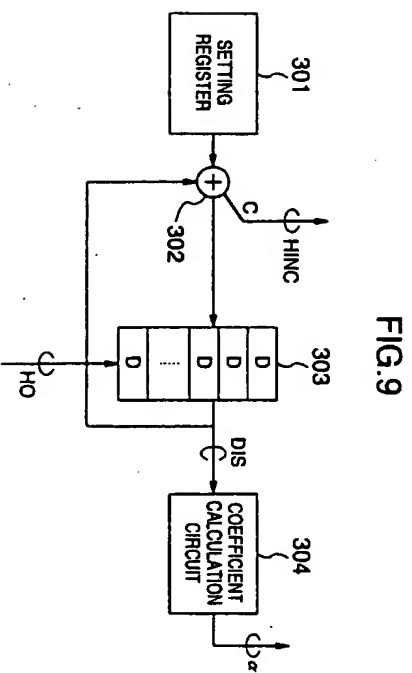


FIG. 9

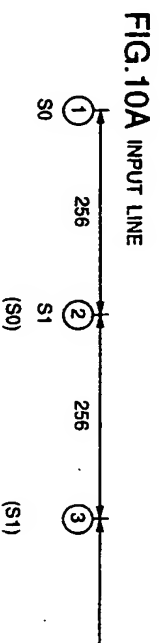


FIG. 10A INPUT LINE

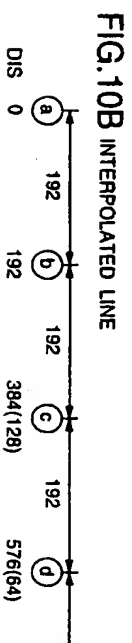


FIG. 10B INTERPOLATED LINE

FIG. 11A

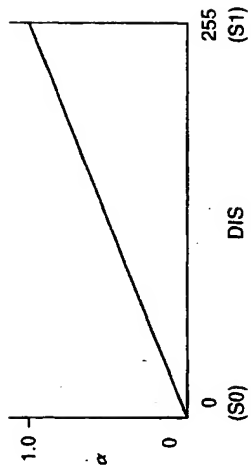


FIG. 11B

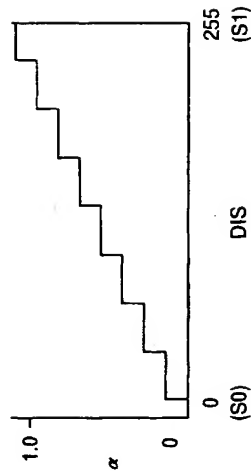


FIG. 11C

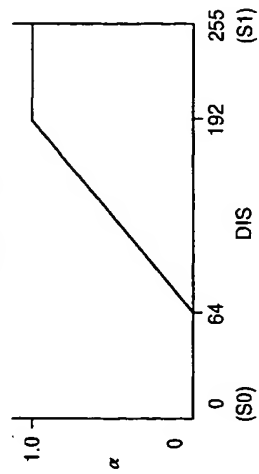


FIG. 11D

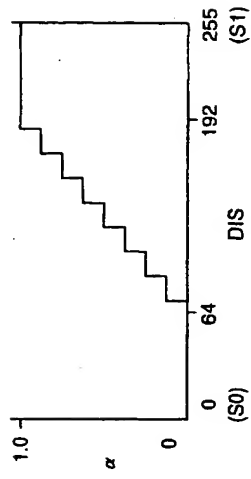


FIG. 12

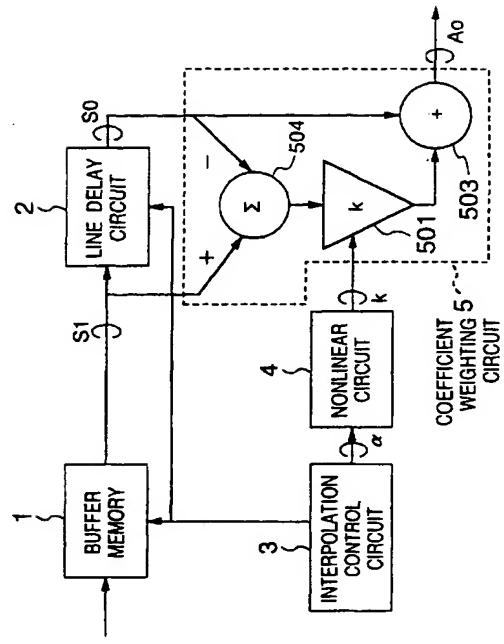


FIG.13

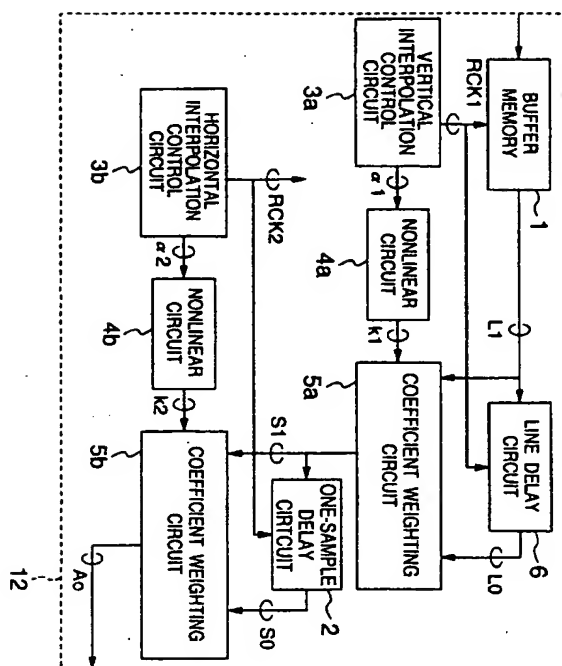


FIG.14

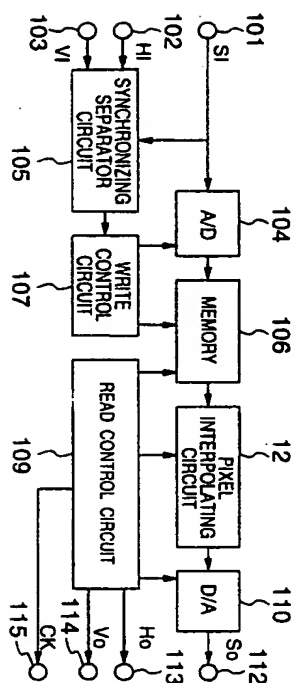


FIG.15

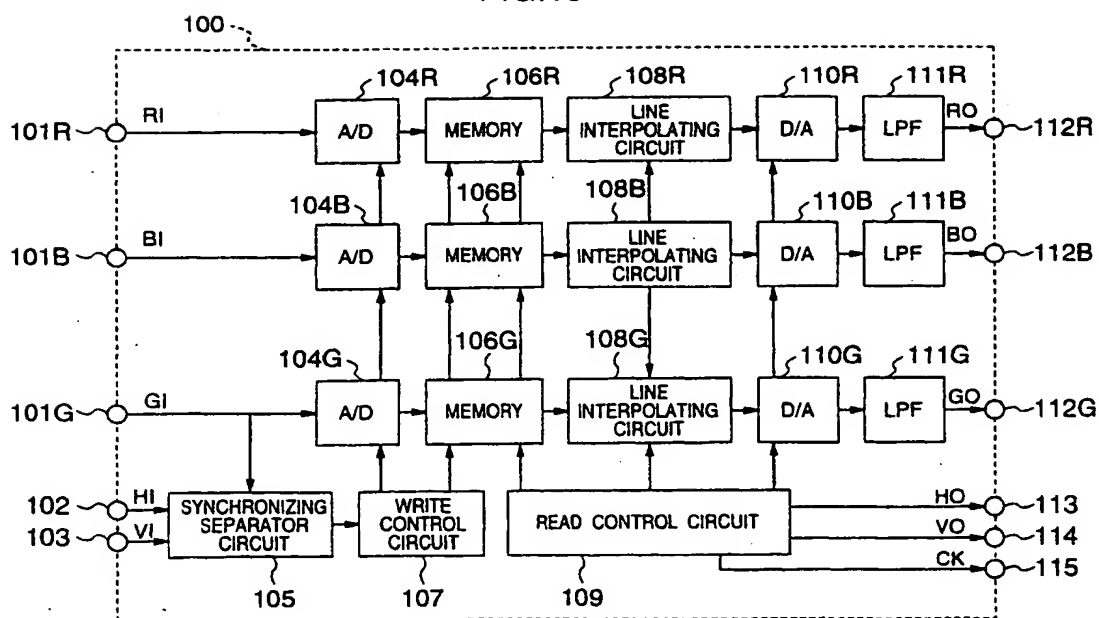


FIG. 16

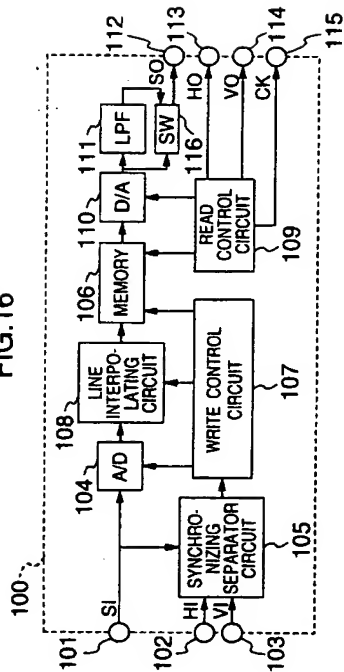


FIG. 17

